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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,950	12/11/2003	David Jia Chen	ROC920030250US1	9248

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EXAMINER	
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ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/732,950	CHEN ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *7 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's affirmation of the election without traverse of claims 1-6 (Group I) in the reply filed on May 26, 2005 is acknowledged.

2. Claims 7-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Suzuki** (5,598,029).

Regarding claim 1:

Suzuki discloses a decoupling capacitor (Fig. 4), comprising:

a fixed resistance in series with said capacitor, said capacitor formed by a polysilicon layer 4 and a diffusion layer (8 and/or 9), said fixed resistance formed by contacts (TH1a,1b,2a,2b, etc.) connecting said polysilicon layer 4 to a first voltage level buss 1 (i.e., power supply line, Col. 4, lines 49-50) and said diffusion layer to a second voltage level buss 2 (i.e., ground line, Col. 4, lines 49-50);

said contacts being of location and capacity for protecting surrounding circuits in the event there is a defect shorting said busses together (i.e., note that all contacts are located "away" from the "inversion layer region" of the substrate under gate oxide 3, see Fig. 4 and Col. 5, lines 27-33; therefore, even if there is a defect in the gate oxide 3, the location of the contacts would protect surrounding circuits because any defect current must pass through the inversion layer region of the substrate where there are no contacts); and

said capacitor able to function at a frequency sufficiently high to suppress noise on said first and second busses to a value which achieves bus stability (note Col. 2, lines 10-16 and Col. 5, lines 24-33). Note that terminology such as "sufficiently high" is relative; accordingly, Suzuki's capacitor is capable of functioning at a "sufficiently high frequency" to suppress noise, since "a sufficiently high frequency" could be any frequency that one chooses to quantify as "sufficiently high".

Suzuki **lacks** specifying defect current or specifically reciting that the contacts are located and capable of limiting defect current. However, as noted above, Suzuki shows (in Fig. 4) that the contacts (TH1a, TH1b, etc.) are located away from the inversion-layer region (underneath gate oxide 3); accordingly, any defect current resulting from a defect in the gate oxide 3 must pass through the inversion-layer region of the substrate in order to short the busses (1, 2) together. Such a construction would obviously limit defect current because the inversion-layer region of the substrate would function as a "defect-current limiter", i.e., if the contacts (e.g., TH1a and TH1b) were separated ONLY by the gate oxide 3, then a defect in the gate oxide could break down the gate oxide 3 such that the contacts are shorted in a manner allowing a large amount of defect current to flow; however, because Suzuki positions the contacts such that they are separated by the gate oxide 3 AND the inversion-layer region, any defect current (caused by a breakdown in gate oxide 3) would still be limited by the inversion-layer region. Therefore, it would have been obvious to one of ordinary skill in the art to modify Suzuki by specifically reciting that the contacts are of location and capacity for limiting defect current. In other words, Suzuki's capacitor provides a structure comprising contacts being located and capable of limiting defect current while suppressing noise at a "sufficiently high frequency". *Regarding claims 2-6:*

Suzuki discloses the contacts (TH1a,1b,2a,2b, etc., note Fig. 4) include a first set of contacts (TH1b, TH2b) to a first voltage (ground) and a second set of contacts (TH1a, TH2a) to a second voltage (power);

a defect leakage current limiting path (e.g., note the "inversion layer" region of the substrate under gate oxide 3, i.e., note Fig. 4 and Col. 5, lines 27-33) including said first set and said second sets of contacts separated by a distance optimized (i.e., this would be any distance,

since an "optimized distance" is relative to one's definition of "optimum" for a given design) to cause a defect shorting said polysilicon layer 4 to said substrate 20 to force defect current to travel from the first set of contacts (TH1b, TH2b) through a section of the substrate (i.e., the "inversion layer"), then to the polysilicon 4 through any defects (in the gate oxide 3), and then along the rest of the polysilicon layer 4 to said second set of contacts (TH1a, TH2a).

Suzuki **lacks** specifying features specified in claims 3-6, including the following: preselected minimum and maximum resistance values, preselected maximum leakage current, preselected decoupling RC factor, total contact resistance being less than 10 % of combined sheet resistance, bandwidth limiting resistance of R/2, technology-dependent number of contacts, etc.. These features (as specified in claims 3-6) are all considered to be generalized statements that are readily attributable to Suzuki's capacitor. In other words, the limitations in the instant claims are all directed to relative terminology, where the relative terms provide no specific, quantifiable, additional structural limitations to a capacitor structure that would patentably distinguish over Suzuki's capacitor structure. For example, claim 4 recites, "*first and second sets of contacts in sufficient number to effectively achieve total contact resistance less than 10% of combined sheet resistance...*". Essentially, this claim does NOT further limit the structure of the capacitor in claim 3, which already has first and second sets of contacts. More specifically, terminology such as "*sufficient number*" and "*total contact resistance less than 10% of total sheet resistance*" can only be interpreted to mean "any number" (i.e., any number can be a "sufficient number") and "any resistance value" (i.e., since the "sheet resistance" has not been quantified and therefore could be any value, "10% of any value" is essentially "any value" that one chooses); therefore, the limitations recited in the instant claims are considered to be general

statements that are readily attributed to Suzuki's capacitor structure. In sum, the instant claims are held obvious over Suzuki because Suzuki's capacitor structure contains all pertinent structural limitations necessary for one of ordinary skill in the art to attribute the generalized features recited in the instant claims.

Remarks

4. Applicants' remarks/arguments have been carefully reviewed and considered, but they are not persuasive. Applicants assert that Suzuki expressly limits the parasitic resistance due to the wiring method and that the fixed resistance formed by the contacts is purely due to the number of contacts (see page 9 of the remarks). In the text referenced by the Applicant (Col. 3, lines 54-56 and Col. 4, lines 4-7), the examiner finds nothing to suggest that the fixed resistance is purely due to the number of contacts, especially because Suzuki states, "[t]he parasitic resistance can be suppressed small by shortening the length and thickening the width of the electrode of the bypass capacitor", i.e., the electrode of the bypass capacitor would be the "gate" electrode 4 shown in Fig. 4 and described in Col. 3, lines 37-39. In any case, as explained in detail above with respect to the rejection of claim 1, Suzuki renders obvious the currently claimed feature of "said contacts being of location and capacity for protecting surrounding circuits...by limiting defect current...".

With respect to the relative terminology used in the claims, it seems from the Applicants' remarks that there is no disagreement with the examiner's position that Suzuki's capacitor structure is able to function at a frequency "sufficiently high" to suppress noise on said first and second busses to a value which achieves bus stability (see Applicants' remarks on page 10).

With respect to Applicants' remarks that Suzuki's capacitor would never be able to "do any of this" (i.e., achieve what the current invention achieves) because there is no protection if the VDD and GND plates were to short together, the examiner maintains that Suzuki's capacitor is capable of providing protection if VDD and GND are shorted by "defect shorting" cause by a defect in the gate oxide 4 (note again Suzuki, Fig. 4). In other words, the "defect shorting" described in the current invention is due to a defect occurring in a gate oxide (note Fig. 10 of the current invention); accordingly, when a similar defect occurs in Suzuki, the capacitor structure would provide protection because the contacts are located away from the gate oxide (as explained above in detail with respect to claim 1).

In sum, the current invention is held obvious over Suzuki (alone) primarily because claims 1-6 are drawn to a decoupling capacitor (emphasis added). The structural limitations of the claimed decoupling capacitor are disclosed by Suzuki, and the features recited in the current claims (that are not specifically disclosed by Suzuki) are considered to be generalized features that could also be recited and attributed to Suzuki's decoupling capacitor because Suzuki discloses all pertinent structural limitations of the claimed decoupling capacitor. With respect to the Applicants' request in accordance with MPEP 707.02 (j) and 707.03, the examiner suggests directing the claim language to specific structural limitations for the decoupling capacitor, e.g., including specific structural limitations as to the location of the contacts with respect to the polysilicon layer, the first voltage buss, the diffusion layer and the second level voltage buss; the location of the contacts with respect to the surrounding circuits being protected; or distances between contacts, sizes of contacts (if relevant), etc.. Such limitations, which are discrete

structural elements (or positional relationship between structural elements), would be considered to have patentable weight since the claims are directed to a decoupling capacitor structure.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

August 16, 2005

MATTHEW SMITH
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